



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/032,863

03/02/1998

GORDON F. GRIGOR

00100.98.1117

1397

23418

7590

09/26/2007

VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

EXAMINER

NGUYEN, KEVIN M

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

09/26/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 09/032,863	Applicant(s) GRIGOR ET AL.	
	Examiner Kevin M. Nguyen	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 13 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 24,29-33,38-53 and 56-59 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 24,29-33,38-53 and 56-59 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Arguments

1. In view of applicant's amendments filed on 7/13/2007 to the claim 33, the rejection of claim 33 under 35 USC 112, second paragraph, stands withdrawn.
2. Applicant's arguments, see pages 13-16, filed on 7/13/2007, with respect to the rejection(s) of claim(s) 24, 29-33, 38-53 and 56-59 under the statutory basis for the previous rejection have been fully considered and are not persuasive.

Applicant argues with respect to claim 24 recited "reconfiguring of multiple displays so that multiple displays are configured in accordance with display preferences when the current configuration can be reconfigured after the computing system and multiple displays have already been configured" found on page 13, these are not found persuasive. Hogle discusses the reconfiguration after two displays have already been configured in column 9, lines 21-42. Hogle further discloses display preferences as corresponding to display characteristics, figs. 8(a)-8(g), col. 11, lines 26-47.

Applicant argues that Hogle does not disclose a single coupling controller found on page 13, these are not found persuasive. Hogle discusses a single forking display driver 201, fig. 6, column 9, lines 47-48.

Applicant argues that Hogle does not disclose a different resolution found on page 13, these are not found persuasive. Hogle discusses this limitation in column 9, lines 31-36.

Applicant argues that Hogle does not disclose a processing unit found on page 14, these are not found persuasive. Hogle discusses a computer which implies a processing unit, col. 5, lines 61-64 or a CPU 304.

Applicant argues with respect to claims 24 and 33 recited "a display controller that simultaneously provides display data to the multiple display and the display controller is coupled to a plurality of screen memories each storing separate display data and the display controller retrieves the display data from the plurality of screen memories" found on page 13, these are not found persuasive. In previous Office action mailed 3/13/2007, the examiner indicated the screen memory at col. 6, line 56 to col. 7, line 5. However, the broad claimed limitation "a plurality of screen memories" further read on Hogle reference. Hogle further teaches two display controllers 36 and 205 which accesses a plurality of portions of screen memory as a bit-depth and the other color of pixel, col. 9, lines 6-16. Hogle further discusses reconfiguration in column 9, lines 6-58. Hogle further discusses display simultaneously in column 10, lines 54-57.

Applicant argues that "the claim requires a single display controller that simultaneously provides display data to the multiple displays" found on page 14, these are not found persuasive. This claimed limitation is not consistent with the figure 1 and specification of the current application. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a single display controller) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification,

limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that “a system of Hogle uses two separate display controllers neither of which have access to the screen memories of the other” found on page 14, these are not found persuasive because the examiner cited two display controllers 36 and 205 to access a plurality of portions of screen memory as a bit-depth and the other color of pixel, col. 9, lines 6-16.

Applicant argues that “claim 59 requires switching device” found on page 14, these are not persuasive. Hogle discloses a forking display driver 201.

Applicant argues that “claim 42 requires screen memories and coupling controller” found on page 15, these are not found persuasive. Hogle discusses Hogle discusses this limitation in col. 9, lines 6-16 that a plurality of portions of screen memory as a bit-depth and the other color of pixel, and a forking display driver 201.

Applicant argues that “claim 42 requires screen memories storing separate display data” found on page 15, these are not found persuasive. Hogle discusses this limitation in col. 9, lines 6-16 that a plurality of portions of screen memory as a bit-depth and the other color of pixel.

For these reasons, the rejection based on Hogle is maintained.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2629

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 24, 29-33, 38-41 and 57-59** are rejected under 35 U.S.C. 102(e) as being anticipated by Hogle, IV (US 5,923,307) hereinafter Hogle.

5. **As to claim 24**, Hogle teaches a video graphics processing circuit (fig. 3) comprises:

- a. a processing unit *[a CPU 304];*
- b. memory *[a memory 302];*
- c. a coupling controller *[a forking display driver 201 as corresponding to the switches such that the desired display drivers 35 and 203 are coupled to two display monitors 37 and 207 via display adapters 36 and 205, fig. 3, col. 9, lines 47-50];*
- d. display preferences *[display characteristics, figs. 8(a)-8(g), col. 11, lines 26-47];*
- e. configuration properties *[display properties, fig. 9(a) through fig. 11(c), col. 11, line 48 through col. 12, line 13];*
- f. multiple display devices *[330 and 332, fig. 3];*
- g. a plurality of display drivers *[35 and 203, fig. 6];*
- h. a plurality of screen memories *[col. 6, line 56—col. 7, line 5];*
- i. display controllers (36 and 205, fig. 6);

- j. programming instructions (a specialized program codes, col. 10, lines 25);
- k. simultaneously displaying display data to the multiple displays (fig. 16a, col. 10, lines 52-56);

the program codes (programming instructions) identify said elements (a)-(k) performing and operating the functions of the configuration of multiple monitors 330 and 332 such as said display characteristics, and additional functions of whether the reconfiguration of multiple monitors 330 and 332 such display properties to be displayed the quality of multiple windows/graphics until satisfy. Each of a plurality of windows/graphics displays the following/software instructions (programming instructions) in the display properties of the control panel window in response to the switching software in real time, in accordance with each of corresponding screen memories is retrieved from the main memory 302 to be executed by the CPU 304 in order to run smoothly and faster without freezing and being slow, figs. 9b, 10a, and 10b, col. 9, and lines 6-20, col. 10, line 16—col. 11—col.12, line 13.

As to claim 29, Hogle teaches the forking display driver 201 in response with the following instructions (programming instructions) in the display properties of the control panel window as corresponding to the switching software such that the desired display drivers 35 and 203 are automatically coupled to two display monitors 37 and 207 via display adapters 36 and 205 in real time, see figs. 9b, 10a, and 10b.

As to claims 31 and 32, Hogle teaches each of a plurality of windows/graphics displaying the following/software instructions (programming instructions) in the display properties of the control panel window in response to the switching software in real time,

each of corresponding screen memories is retrieved from the main memory 302 to be executed by the CPU 304 in order to run smoothly and faster without freezing and being slow, figs. 9b, 10a, and 10b, col. 9, and lines 6-20.

As to claim 30, Hogle teaches the forking display driver 201 in response with the following instructions (programming instructions) in the display properties of the control panel window as corresponding to the switching software such that the desired display drivers 35 and 203 are automatically coupled to three display monitors via display adapters 36 and 205 in real time, see figs. 9b, 10a, 10b, and 17a.

6. The limitation of **claim 33** is similar to those of claim 24, though in a **digital storage medium** executed by a processing unit, therefore the rejection of claim 33 will be treated using the same rationale as claim 24.

7. Claim 38 shares the same limitations as those of claim 29 and therefore the rationale for rejection will be the same.

8. Claim 39 shares the same limitations as those of claim 30 and therefore the rationale for rejection will be the same.

9. Claim 40 shares the same limitations as those of claim 31 and therefore the rationale for rejection will be the same.

10. Claim 41 shares the same limitations as those of claim 32 and therefore the rationale for rejection will be the same.

11. As to **claim 57**, Hogle teaches a video graphics processing circuit (fig. 3) comprises:

a processing unit [*a CPU 304*];

memory *[a memory 302];*

a coupling controller *[a forking display driver 201 as corresponding to the switches such that the desired display drivers 35 and 203 are coupled to two display monitors 37 and 207 via display adapters 36 and 205, fig. 3, col. 9, lines 47-50];*

display preferences *[display characteristics, figs. 8(a)-8(g), col. 11, lines 26-47];*

configuration properties *[display properties, fig. 9(a) through fig. 11(c), col. 11, line 48 through col. 12, line 13];*

multiple display devices *[330 and 332, fig. 3];*

programming instructions (a specialized program codes, col. 10, lines 25);

the program codes (programming instructions) identify said elements performing and operating the functions of the configuration of multiple monitors 330 and 332 such as said display characteristics, and additional functions of whether the reconfiguration of multiple monitors 330 and 332 such display properties to be displayed the quality of multiple windows/graphics until satisfy. Each of a plurality of windows/graphics displays the following/software instructions (programming instructions) in the display properties of the control panel window in response to the switching software in real time, in accordance with each of corresponding screen memories is retrieved from the main memory 302 to be executed by the CPU 304 in order to run smoothly and faster without freezing and being slow, figs. 9b, 10a, and 10b, col. 9, and lines 6-20, col. 10, line 16—col. 11—col.12, line 13.

12. As to **claim 58**, the limitation of claim 58 are similar to those of claim 57 though in **method** form without the claimed limitation “a video graphic card, a processing unit, a

Art Unit: 2629

memory stores program instructions, and a coupling controller", therefore the rejection of claim 58, will be treated using the same rationale as claim 57.

As to claim 59, the method of claim 58 comprising switches to couple different screen memories with different controllers to output display data to the multiples displays, whereas Hogle teaches each of a plurality of windows/graphics displaying the following/software instructions (programming instructions) in the display properties of the control panel window in response to the switching software in real time, each of corresponding screen memories is retrieved from the main memory 302 to be executed by the CPU 304 in order to run smoothly and faster without freezing and being slow, figs. 9b, 10a, and 10b, col. 9, and lines 6-20.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. **Claims 42-53 and 56** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogle, IV (US 5,923,307) hereinafter Hogle in view of Wong et al (US 5,963,192) hereinafter Wong.

15. As to **claim 42**, Hogle teaches a video graphics processing circuit (fig. 3) comprises:

a plurality of drivers (35 and 203 fig. 6);

memory [*a memory 302*];

Art Unit: 2629

screen memory, col. 6, lines 56—col. 7, line 5;

a coupling controller *[a forking display driver 201 as corresponding to the switches such that the desired display drivers 35 and 203 are coupled to two display monitors 37 and 207 via display adapters 36 and 205, fig. 3, col. 9, lines 47-50];*

display preferences *[the details of display characteristics, figs. 8(a)-8(g), col. 11, lines 26-47];*

configuration properties *[display properties, fig. 9(a) through fig. 11(c), col. 11, line 48 through col. 12, line 13];*

multiple display devices *[330 and 332, fig. 3];*

a plurality of display drivers *[35 and 203, fig. 6];*

a plurality of screen memories *[col. 6, line 56—col. 7, line 5];*

display controllers (36 and 205, fig. 6);

programming instructions (a specialized program codes, col. 10, lines 25);

simultaneously displaying display data to the multiple displays (fig. 16a, col. 10, lines 52-56);

the program codes (programming instructions) identify said elements performing and operating the functions of the configuration of multiple monitors 330 and 332 such as said display characteristics, and additional functions of whether the reconfiguration of multiple monitors 330 and 332 such display properties to be displayed the quality of multiple windows/graphics until satisfy. Each of a plurality of windows/graphics displays the following/software instructions (programming instructions) in the display properties of the control panel window in response to the switching software in real time, in

Art Unit: 2629

accordance with each of corresponding screen memories is retrieved from the main memory 302 to be executed by the CPU 304 in order to run smoothly and faster without freezing and being slow, figs. 9b, 10a, and 10b, col. 9, and lines 6-20, col. 10, line 16—col. 11—col.12, line 13.

Accordingly, Hogle teaches all of the claimed limitation, except for a plurality of display controllers included on a single video graphics card.

However, Wong teaches a single video card 12 comprising a display processor 40 (corresponding to a first display controller) and a display processor 42 (corresponding to a second display controller) are arranged on said single video card 12 thereof in fig. 2.

As to claim 43, the video graphics processing circuit of claim 42, further comprises a graphics engine, whereas Hogle teaches a graphics engine which is a graphic device 34, fig. 6.

As to claim 44, the video graphics processing circuit of claim 42, further comprises a user interface, whereas Hogle discloses a graphical user interface (GUI) 31, fig. 6.

As to claim 45, Hogle teaches at least of a plurality of windows/graphics displaying the following/software instructions (operational rules) in the display properties of the control panel window in response to the switching software in real time, each of corresponding screen memories is retrieved from the main memory 302 to be executed by the CPU 304 in order to run smoothly and faster without freezing and being slow, figs. 9b, 10a, and 10b, col. 9, and lines 6-20.

As to claim 46, Hogle teaches each of a plurality of windows/graphics displaying the following/software instructions (programming instructions) in the display properties of the control panel window in response to the switching software in real time, each of corresponding screen memories is retrieved from the main memory 302 to be executed by the CPU 304 in order to run smoothly and faster without freezing and being slow, figs. 9b, 10a, and 10b, col. 9, and lines 6-20.

As to claim 47, Hogle teaches the forking display driver 201 in response with the following instructions (programming instructions) in the display properties of the control panel window as corresponding to the switching software such that the desired display drivers 35 and 203 are automatically coupled to three display monitors via display adapters 36 and 205 in real time, see figs. 9b, 10a, 10b, and 17a.

As to claim 48, Hogle teaches each of a plurality of windows/graphics displaying the following/software instructions (programming instructions) in the display properties of the control panel window in response to the switching software in real time, each of corresponding screen memories is retrieved from the main memory 302 to be executed by the CPU 304 in order to run smoothly and faster without freezing and being slow, figs. 9b, 10a, and 10b, col. 9, and lines 6-20.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Wong into Hogle to create the claimed invention. It would have been obvious to modify Hogle to form the display processor 40 and the display processor 42 on a common video card 12 as taught by Wong, because this would improve the quality of the image being displayed without flickering, while

Art Unit: 2629

eliminating full line buffers result in a saving of approximately 30,000 transistors per buffer and a corresponding reduction in operating power (see Wong's abstract).

16. As to **claim 49**, Hogle teaches a video graphics processing circuit (fig. 3) comprises:

screen memory, col. 6, lines 56—col. 7, line 5;

a plurality of drivers (35 and 203 fig. 6);

a coupling module (*a switching software in which a forking display driver 201 programmability coupled to the desired display drivers 35 and 203 and two display monitors 37 and 207 via display adapters 36 and 205, fig. 3, col. 9, lines 47-50*);

a coupling controller [*a forking display driver 201 as corresponding to the physical switch such that the desired display drivers 35 and 203 are coupled to two display monitors 37 and 207 via display adapters 36 and 205, fig. 3, col. 9, lines 47-50*];

configuration properties [display properties, fig. 9(a) through fig. 11(c), col. 11, line 48 through col. 12, line 13];

a plurality of display drivers [*35 and 203, fig. 6*];

simultaneously displaying display data to the multiple displays (fig. 16a, col. 10, lines 52-56);

the program codes (programming instructions) identify said elements (304, 302, 201, 330, 332) performing and operating the functions of the configuration of multiple monitors 330 and 332 such as said display characteristics, and additional functions of whether the reconfiguration of multiple monitors 330 and 332 such display properties to be displayed the quality of multiple windows/graphics until satisfy. Each of a plurality of

Art Unit: 2629

windows/graphics displays the following/software instructions (programming instructions) in the display properties of the control panel window in response to the switching software in real time, in accordance with each of corresponding screen memories is retrieved from the main memory 302 to be executed by the CPU 304 in order to run smoothly and faster without freezing and being slow, figs. 9b, 10a, and 10b, col. 9, and lines 6-20, col. 10, line 16—col. 11—col.12, line 13.

Accordingly, Hogle teaches all of the claimed limitation, except for a plurality of display controllers included on a single video graphics card.

However, Wong teaches a single video card 12 comprising a display processor 40 (corresponding to a first display controller) and a display processor 42 (corresponding to a second display controller) is arranged on said single video card 12 thereof in fig. 2.

As to claim 50, the method of claim 49 comprising switches to couple different screen memories with different controllers to output display data to the multiples displays, whereas Hogle teaches the forking display driver 201 as corresponding to the physical switches such that the desired display drivers 35 and 203 are automatically coupled to two display monitors 37 and 207 via display adapters 36 and 205 in real time.

As to claim 51, Hogle teaches GUI 31 coupling to the forking display driver 201.

As to claim 52, Hogle teaches screen memory in col. 6, lines 56-col. 7, line 5, and col. 9, lines 6-20.

As to claim 53, figs. 9b, 10a, and 10b of Hogle show the display properties in the control panel window, which identify the desired displays.

As to claim 56, Hogle teaches dual image of the object appears simultaneously on monitors 1 and 2, col. 10, lines 54-56.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Wong into Hogle to create the claimed invention. It would have been obvious to modify Hogle to form the display processor 40 and the display processor 42 on a common video card 12 as taught by Wong, because this would improve the quality of the image being displayed without flickering, while eliminating full line buffers result in a saving of approximately 30,000 transistors per buffer and a corresponding reduction in operating power (see Wong's abstract).

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Art Unit: 2629


Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. NGUYEN whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, a supervisor RICHARD A. HJERPE can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see <http://portal.uspto.gov/external/portal/pair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Nguyen
Patent Examiner
Art Unit 2629

KMN
September 19, 2007



RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNICAL CENTER 2600